UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,288	04/20/2004	Kazuo Sakamoto	XA-10084	2625

181 7590 06/02/2008

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
06/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
sstiles@milesstockbridge.com

Office Action Summary	Application No.	Applicant(s)	
	10/827,288	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	FAHMIDA RAHMAN	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,7-10 and 13* is/are allowed.

6)☒ Claim(s) *1-3,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 2/21/08.

2. Claims 1, 3-4, 9-11 have been amended.

3. Claims 12 and 13 have been added.

4. Claims 5-6 have been canceled.

5. Thus, claims 1-4, 7-13 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of Moss et al (US Patent 6917561).

For claim 1, Schaefer teaches the following limitations:

A data processing device (140, 120, 122, 124 in Fig 1) formed as a semiconductor integrated circuit, which is coupled to a device (112) for performing data transmission and reception (112 is a memory that transmits and receives data), said data processing device comprising: a central processing unit (140); an interface unit (200 and the clock distribution network to DQ buffers) for

data transmission and reception to and from the device, wherein said interface unit includes: an external terminal (terminal for CLKD in Fig 2) for outputting a clock signal; an output driver for driving said external terminal to output said clock signal (the wires connecting CLKD to 212a-212i in Fig 2 form clock distribution network and can be considered as output driver as the network is driving the terminal to provide clock to DQ buffers); a load circuit (210, 204, 206, 208) capable of imparting, to the clock signal (202) extracted from a position in a stage previous to output driver in a clock signal path (210 extracting signal just before CLKD in Fig 2), a variable delay ([0005] mentions that delay compensation circuit compensate for variations in process temperature, loading conditions. Thus, circuitry within 200 incorporates a variable delay) in accordance with a delay (delay = B) resulting from an external load (DQ buffers shown in 212a-212i) coupled to external terminal in order to generate a delayed clock signal (CLKD is a delayed signal).

For the limitations, "an external data input terminal for inputting data; and a latch circuit for latching data in accordance with said delayed clock signal.", Schaefer has external data input terminal (D0, D1 in Fig 2) for inputting data and a data latch circuit (212a) for latching said external data in accordance with said delayed signal (data is latched 212a according to delayed signal CLKD), although the data terminal and data latch circuit are not within 200, or the interface circuit. Besides, device 112 is not an external device. Instead, it is internal to 110.

Moss et al teaches a system where memory device is external to memory controller (Fig 1). The memory controller, or the interface unit (10 in Fig 1), comprises an external data input terminal (DQ_IN) for inputting external data (Fig 1); and a data latch circuit (30) for latching said external data in accordance with said delayed clock signal (22 is the delayed clock signal. 30 latches data in accordance with delayed clock 22).

Although 112, a DRAM memory array ([0013]), is shown within 110 in Schaefer, it can be placed as an external unit as DRAM can be a stand alone device in an integrated circuit as shown in Moss (Fig 1).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer and Moss, as memory device is typically located external to memory controller and data latch is provided in interface circuit for better synchronization.

For claim 12, 210 extracts CLKD from a stage immediately preceding said output driver as shown in Fig 2.

7. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of

Moss et al (US Patent 6917561), further in view of Grossnickle et al (US Patent Application Publication 2004/0064749).

For claims 2, 3, Schaefer and Moss do not teach that the load circuit is a time constant circuit comprising resistors and capacitors.

Grossnickle et al teach the delay circuit comprising resistors (P1301) and capacitors (CAP0-CAP3). Fig 3 shows the delay circuit comprising time constant circuits for generating signals with different amounts of delay. Grossnickle et al generate plurality of clock signals with different amount of delay ([0027] mentions that clock generators and delay lock loops use delay elements to manipulate clock edges. Thus, clock generators, DLLs generate plurality of delayed clock signals). Clock signals are typically used to latch data in memory, buffers, registers and other storage units, where any of the clock signals generated from clock generators, DLL, PLL can be selected for latching data inputted from external device.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer, Moss and Grossnickle. One ordinary skill in the art would be motivated to have the time constant circuits as taught by Grossnickle in the system of Schaefer to tune the delay settings.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent Application Publication 2005/0243635), in view of Moss et al (US Patent 6917561), further in view of Strub et al (US Patent Application Publication 2004/0156616).

For claim 11, Schaefer teaches the data processing device as stated above. In addition, Schaefer teaches memory array 112 coupled to data processing device that performs data transmission and reception based on clock signal outputted from external terminal of said data signal. However, Schaefer does not teach any non-volatile storage as 112 is a DDR ([0013]).

Strub et al teach a non-volatile storage device that is controlled by DDR ([0141] of page 18). Therefore, non-volatile storage is based on DDR, which in turn based on clock signal outputted from external terminal of said data processing device. Thus, non-volatile storage is based on clock signal outputted from external terminal of said data processing device.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer, Moss and Strub et al. One ordinary skill would be motivated to control non-volatile through DDR, since that can effect in power saving ([0141] in Strub et al).

Response to Arguments

Applicant's arguments filed on 2/21/08 have been considered but are moot in view of the new ground(s) of rejection. As Schaefer is still relied upon for rejection, Examiner is addressing arguments regarding Schaefer.

Applicant argues that the clock output in Schaefer is internal, not external. Examiner disagrees, as clock output is external with respect to interface unit as shown in Fig 2. The dotted area is the interface unit and therefore, CLKD is the external clock output terminal.

Allowable Subject Matter

Claims 4, 7-10, 13 are allowed.

Conclusion

The following is a statement of reasons for the indication of allowable subject matter: Claim 4 requires interface unit to include plurality of data input terminals for receiving data from external memory and a plurality of latch circuits for latching the received data based on delayed clock signal. Neither Schaefer nor Moss teaches that the interface unit receives data from external memory. Moss's interface unit 10 receives data, but not from external memory 12.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAHMIDA RAHMAN whose telephone number is (571)272-8159. The examiner can normally be reached on Monday through Friday 8:30 -6:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

/Nitin C. Patel/
Primary Examiner, Art Unit 2116